REMARKS

The Examiner objected to claims 23-28 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter and have rewritten claims 23, 25, 26, and 28 in independent form.

The Examiner rejected claims 1-16 under 35 U.S.C. §102(e) as allegedly being anticipated by Bohr (U.S. Patent No. 6,617,681).

Applicants respectfully traverse the §102(e) rejections with the following arguments.

35 U.S.C. §102(e)

Claims 1-10

The Examiner rejected claims 1-10 under 35 U.S.C. §102(e) as allegedly being anticipated by Bohr (U.S. Patent No. 6,617,681).

Applicants respectfully contend that Bohr does not anticipate claim 1, because Bohr does not teach each and every feature of claim 1.

As first example why Bohr does not teach each and every feature of claim 1, Bohr does not teach the first feature: "predefined block of functional circuitry having a plurality of **I/O pins**" (emphasis added). The Examiner's allegation that the interconnections 118 are I/O pins is not supported in Bohr. While a pin is an interconnection, an interconnection is not inherently a pin. A pin is only one of several types of interconnections and there is no teaching in Bohr that the interconnections 118 are pins. In fact, the Examiner has not even offered an argument to support the Examiner's allegation that the interconnections 118 are pins.

As second example why Bohr does not teach each and every feature of claim 1, Bohr does not teach the second feature: "a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit". Although the Examiner alleges that FIGS. 4 and 6 of Bohr show a backside I/O pad, the Examiner has not identified any structure in FIGS. 4 and 6 of Bohr as a backside I/O pad. Therefore the Examiner has made an allegation without any supporting argument that FIGS. 4 and 6 of Bohr show a backside I/O pad.

Furthermore with respect to said second feature of claim 1, the Examiner alleges that in Bohr, the interconnections 118 are I/O pins and the deep-via 122 is a backside via. However, the

only electrically conductive structure in FIGS. 4 and 6 that is connected to the interconnections 118 through the deep-via 122 is the solder ball 110. Since the solder ball 110 is not a backside I/O pad, as required by claim 1, it is thus clear that Bohr does not teach the second feature of claim 1 even if the interconnections 118 are I/O pins and the deep-via 122 is a backside via.

In addition, the Examiner alleges that: the transistors 140 of FIG. 6 are the functional circuitry of claim 1, the interconnections 118 of FIG. 4 are the I/O pins of claim 1, and the deep-via 122 of FIG. 4 is the backside vias of claim 1. Accordingly, Applicants respectfully contend that the Examiner has improperly combined FIGS. 4 and 6 of Bohr, inasmuch as FIGS. 4 and 6 represent two distinct embodiments and are not disclosed by Bohr as combinable. In effect FIGS. 4 and 6 of Bohr are two distinct references which cannot be legally combined in a rejection under 35 U.S.C. §102(e).

Based on the preceding arguments, Applicants respectfully maintain that Bohr does not anticipate claim 1, and that claim 1 is in condition for allowance.

Since claims 2-10 depend from claim 1, Applicants contend that claims 2-10 are likewise in condition for allowance.

In addition with respect to claims 7 and 9-10, Applicants maintain that neither FIG. 4 nor FIG. 6 show both backside I/O pads and frontside I/O pads.

Claims 11-16

The Examiner rejected claims 11-16 under 35 U.S.C. §102(e) as allegedly being anticipated by Bohr (U.S. Patent No. 6,617,681).

Applicants respectfully contend that Bohr does not anticipate claim 11, because Bohr

does not teach each and every feature of claim 11.

As first example why Bohr does not teach each and every feature of claim 11, Bohr does not teach the first feature: "providing a predefined block of functional circuitry having a plurality of **I/O pins**" (emphasis added). The Examiner's allegation that the interconnections 118 are I/O pins is not supported in Bohr. While a pin is an interconnection, an interconnection is not inherently a pin. A pin is only one of several types of interconnections and there is no teaching in Bohr that the interconnections 118 are pins. In fact, the Examiner has not even offered an argument to support the Examiner's allegation that the interconnections 118 are pins.

As second example why Bohr does not teach each and every feature of claim 11, Bohr does not teach the second feature: "connecting a backside I/O pad electrically to each I/O pin through a backside via of the integrated circuit". Although the Examiner alleges that FIGS. 4 and 6 of Bohr show a backside I/O pad, the Examiner has not identified any structure in FIGS. 4 and 6 of Bohr as a backside I/O pad. Therefore the Examiner has made an allegation without any supporting argument that FIGS. 4 and 6 of Bohr show a backside I/O pad.

Furthermore with respect to said second feature of claim 11, the Examiner alleges that in Bohr, the interconnections 118 are I/O pins and the deep-via 122 is a backside via. However, the only electrically conductive structure in FIGS. 4 and 6 that is connected to the interconnections 118 through the deep-via 122 is the solder ball 110. Since the solder ball 110 is not a backside I/O pad, as required by claim 1, it is thus clear that Bohr does not teach the second feature of claim 11 even if the interconnections 118 are I/O pins and the deep-via 122 is a backside via.

In addition, the Examiner alleges that: the transistors 140 of FIG. 6 are the functional circuitry of claim 11, the interconnections 118 of FIG. 4 are the I/O pins of claim 11, and the

deep-via 122 of FIG. 4 is the backside vias of claim 11. Accordingly, Applicants respectfully contend that the Examiner has improperly combined FIGS. 4 and 6 of Bohr, inasmuch as FIGS. 4 and 6 represent two distinct embodiments and are not disclosed by Bohr as combinable. In effect FIGS. 4 and 6 of Bohr are two distinct references which cannot be legally combined in a rejection under 35 U.S.C. §102(e).

Based on the preceding arguments, Applicants respectfully maintain that Bohr does not anticipate claim 11, and that claim 11 is in condition for allowance.

Since claims 12-16 depend from claim 11, Applicants contend that claims 12-16 are likewise in condition for allowance.

In addition with respect to claims 12 and 14-15, Applicants maintain that neither FIG. 4 nor FIG. 6 show both backside I/O pads and a frontside I/O pad.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account No. 09-0456.

Date: 09/09/2004

Jack P. Friedman
Jack P. Friedman
Registration No. 44,688

Schmeiser, Olsen & Watts
3 Lear Jet Lane, Suite 201
Latham, New York 12110
(518) 220-1850